

FIG. 1

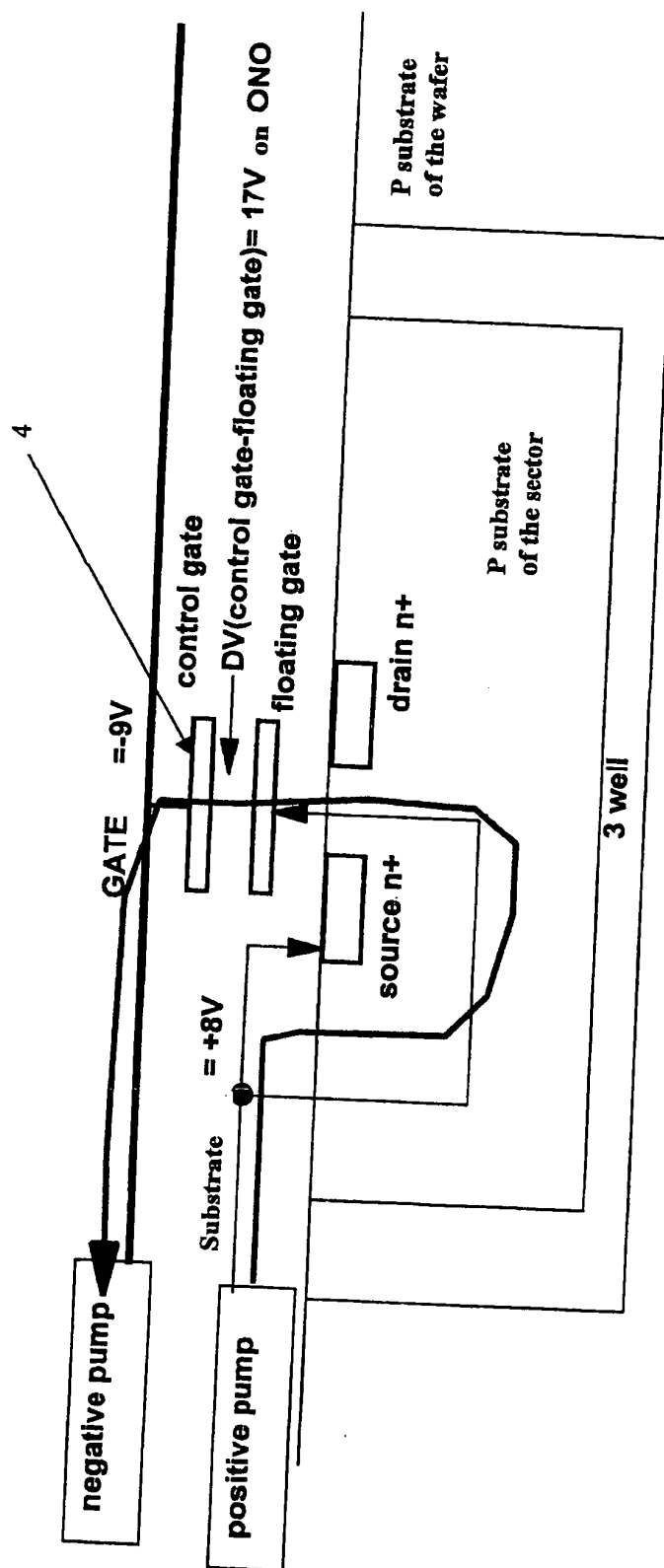


FIG. 2

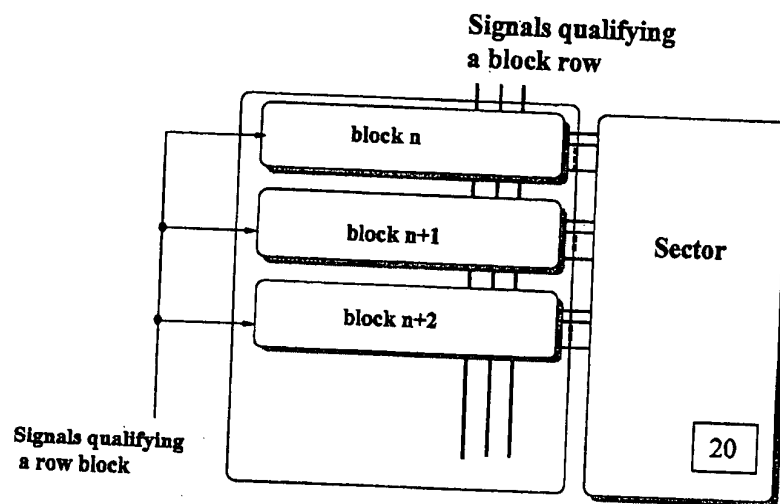


FIG. 3

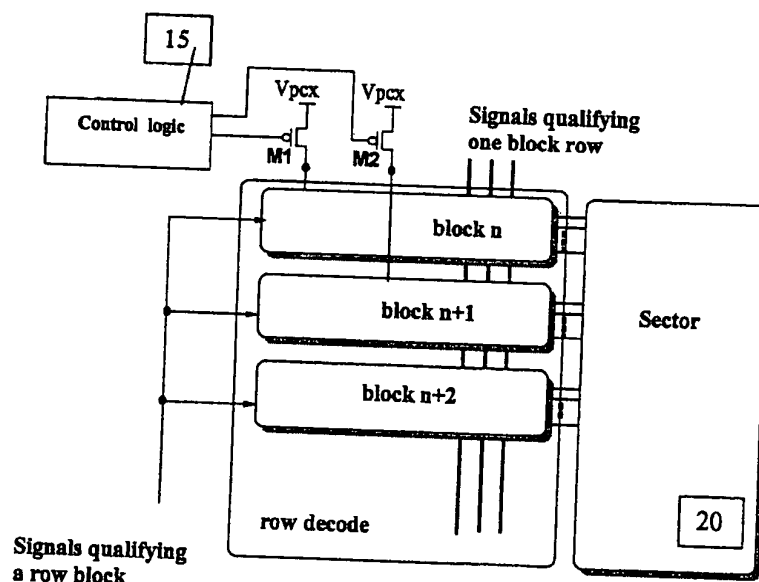


FIG. 4

Title: METHOD FOR DETECTING A RESISTIVE PATH OR A PREDETERMINED POTENTIAL
IN NON-VOLATILE MEMORY ELECTRONIC DEVICES
Inventor(s): Giovanni Campardo et al. Express Mail No. EV336610801US Docket No. 856063.746

FIG. 6

The diagram illustrates the HVNEG control logic. A 'Control logic' block is connected to transistors M1 and M2, which are controlled by Vpcx signals. These transistors drive a stack of three blocks labeled 'block n', 'block n+1', and 'block n+2'. The blocks are connected to a 'Sector' block. Transistors M3 and M4 are connected to the bottom of the block stack and are controlled by HVNEG signals. The diagram also shows 'Signals qualifying one block row' and 'Signals qualifying one row block'.

FIG. 5

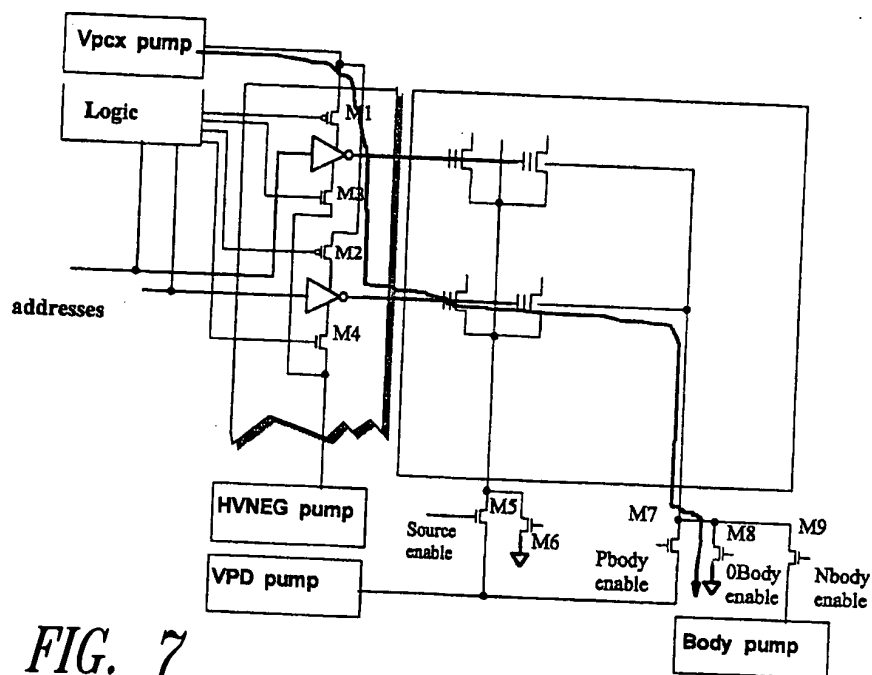


FIG. 7

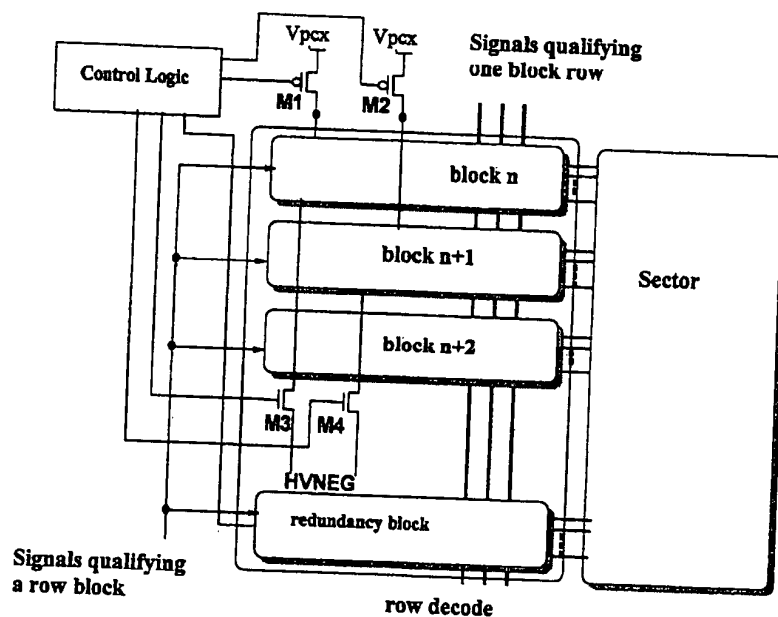
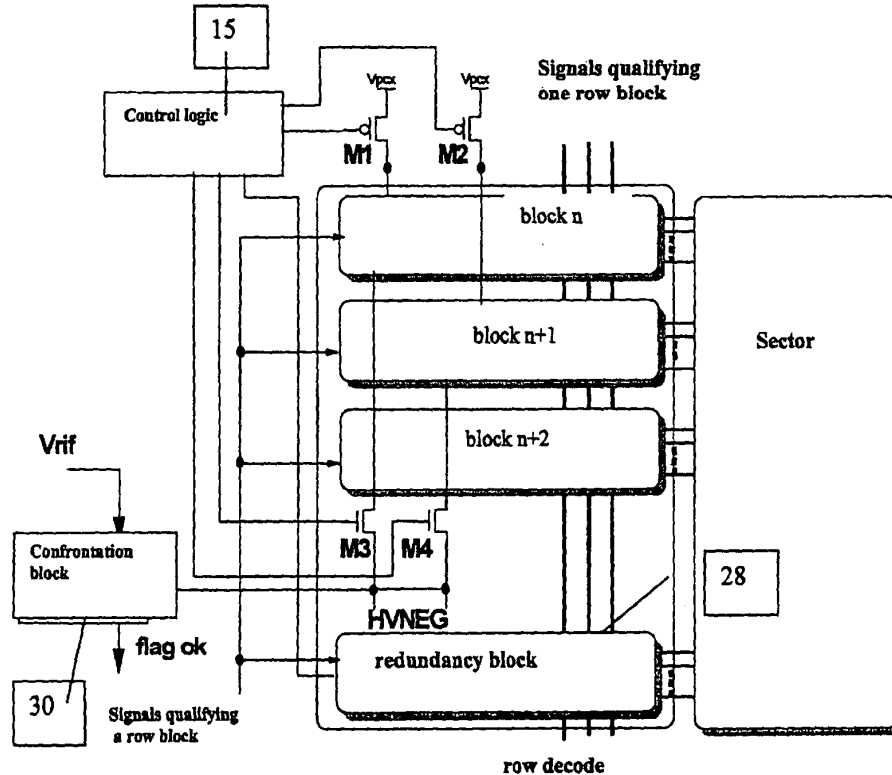
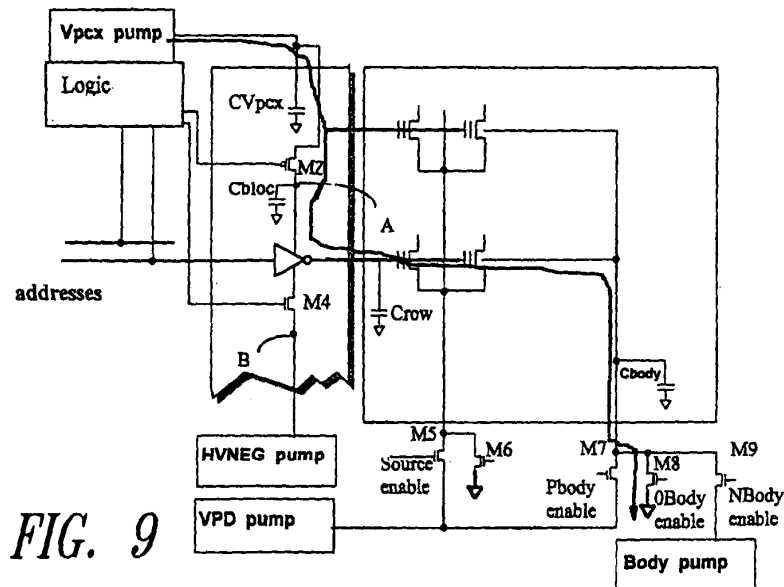


FIG. 8

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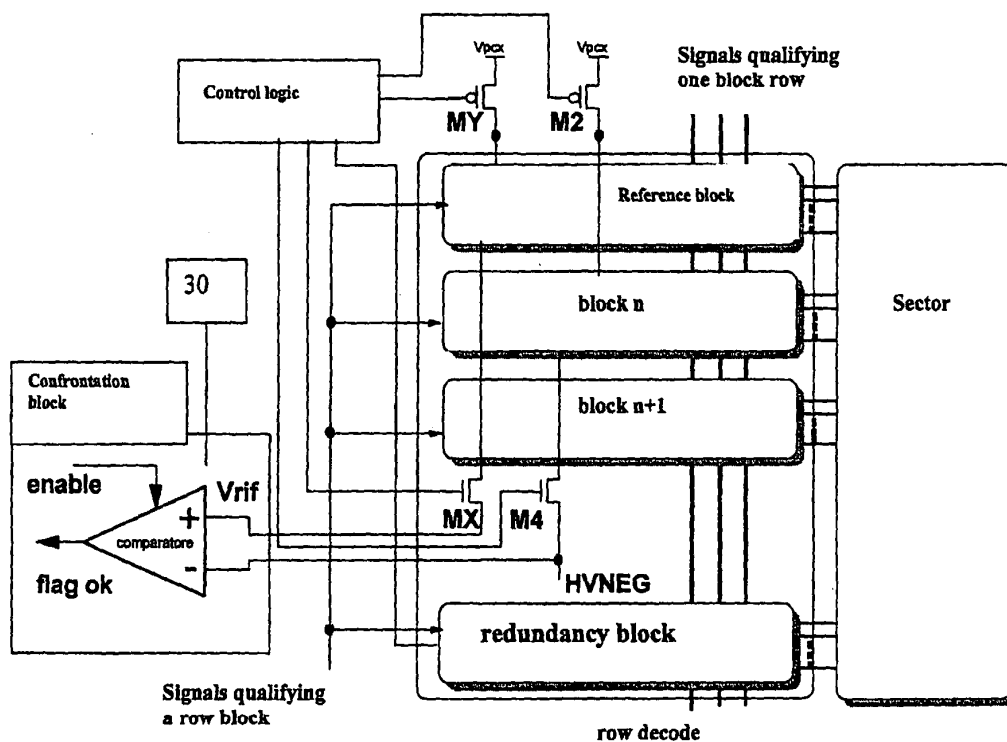


FIG. 11

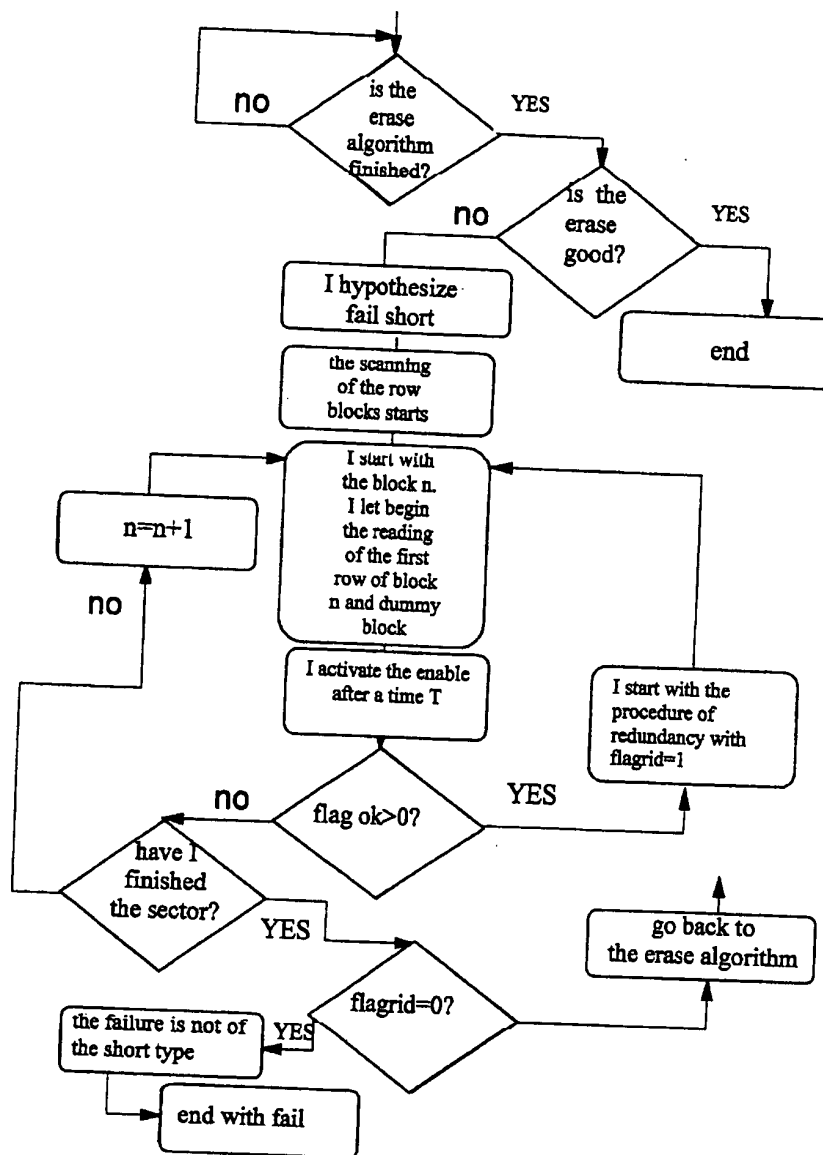


FIG. 12